GTEC UPS MODEL:

LP120 1000/1500/2000 Series

SERVICE MANUAL

www.gtec-power.eu

1.0 Revision Summary

REVISION	SECTION	DESCRIPTION
Rev. A		Formal Release

Table of Contents

1 Introduction

LP120series is a line interactive power system that has sine wave output. It prevents impulse, surge, sag and power outage situations. It provides the UPS output load with a reliable source. It has the following functions:

1.1 Boost:

If the utility voltage drops to line boost activated point*, the AVR will be activated and increase the input voltage by 1.18 times of incoming utility voltage.
*Boost activated point

110 VAC	120 VAC	220 VAC	230 VAC	240 VAC
99 VAC	108 VAC	198 VAC	207 VAC	216 VAC

1.2 Buck:

If the utility voltage reaches to line buck activated point, the AVR will be activated and decrease the input voltage by 0.85 times of incoming utility voltage.
*Buck activated point

110 VAC	120 VAC	220 VAC	230 VAC	240 VAC
121 VAC	132VAC	242 VAC	253 VAC	264VAC

1.3 50/60Hz Automatic Frequency Selection:

The output frequency will automatically match the input frequency (50 or 60Hz).

1.4 Communication Port (USB):

It provides remote shutdown capability via communication port for connected computers.

1.5 Data line/telephone line protection:

The unit provides RJ11 port to provide transient voltage surge suppression (TVSS) for data line or telephone line.

1.6 Cold start (DC start):

The UPS is equipped with DC start function to turn on the UPS without input source.

This manual contains block diagram, principle of operation, system outline and troubleshooting.

2 Block Diagram

The block diagram of LP120series (refer to Figure S-1) is divided into the following parts:

2.1 Main Relay (MAIN-RY):

It's to switch the UPS between line mode and battery mode.

2.2 Boost Relay (BOOST-RY):

At line mode, this is a switch used to boost UPS output voltage 18% when the utility voltage is under line boost activated point. (Refer to boost activated point table in Page 4)
Relay OFF: line voltage is normal
Relay ON: line voltage is under line boost activated point.

2.3 Buck Relay:

At line mode, this is a switch used to lower UPS output voltage 15% when the utility voltage is over line buck activated point. (Refer to buck activated point table in Page4)
Relay OFF: line voltage is normal
Relay ON: line voltage is over line buck activated point

2.4 Main Transformer (MAIN TX):

The Main transformer has three functions:

2.4.1 Inverter Transformer

It provides voltage to UPS output and performs a full-bridge transformer when UPS is at battery mode.

2.4.2 Boost/Buck

The output coils have an output ratio. Thus the output voltage at boost mode is given by (Boost Relay ON):
$V_{OUT} = V_{IN} * 1.18$

The Buck relay is ON when the utility voltage is beyond line buck activated point. It can lower 15% of input voltage:
$V_{OUT} = V_{IN} * 0.85$

2.4.3 Charger:

The battery is charged by the mains through transformer and full-bridge inverter.

2.5 Line Sense

The MCU detects the mains by input voltage and frequency signals converted from the amplifier.

2.6 CPU (PREESCALE/ MC9S08AC48)

The Central Process Unit

2.7 Electricity Switch

It controls the ±12Vdc, +5Vdc, ±6V-BLN supplies.

2.8 Charger:

The source for the Charger comes from the mains through the transformer and full-bridge inverter. The charger is controlled with high frequency technology and the acceptable charging voltage is 13.6~13.9V.

2.9 Inverter Circuit:

The inverter circuit is based on a full-bridge circuitry.

2.10 Interface Circuit:

The UPS display device contains one LCD and one switch.

2.11 Batteries:

Acts as a power supply source while the UPS is on battery mode. Different types of batteries are used for different models of UPS:

750VA: 12V9Ah *1pc or equal capability
1000VA: 12V7Ah *2 pc or equal capability
1500VA: 12V9Ah *2 pc or equal capability
2000VA: 12V10Ah *2 pc or equal capability

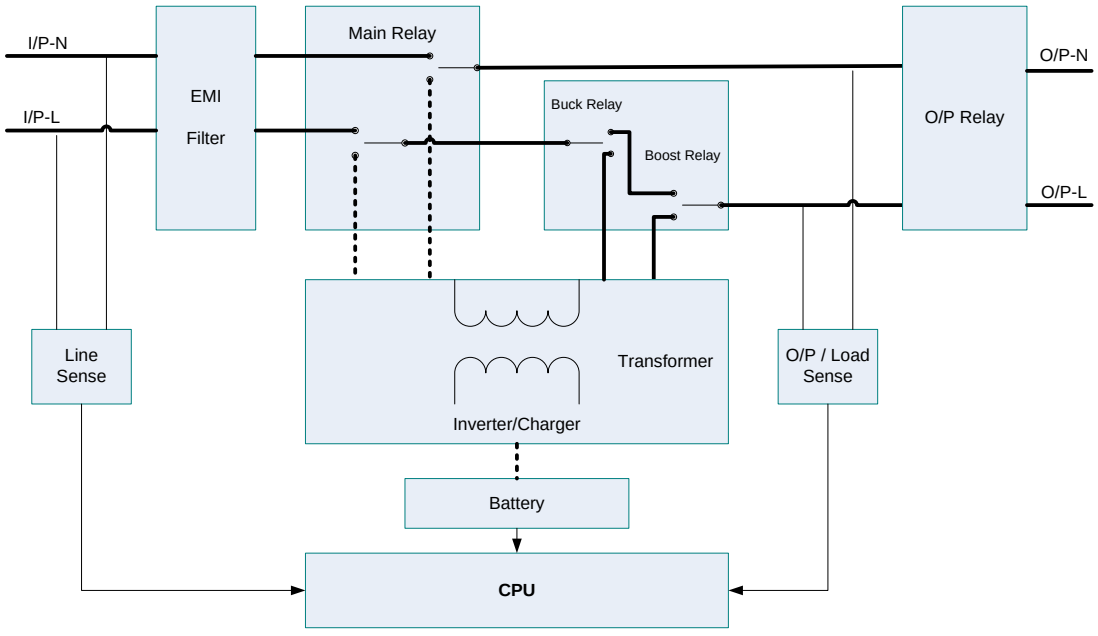


Figure S-1 Block Diagram

3 Control power circuit

The control power (±12Vdc, +5Vdc, ±6V-BLN) comes from the following sources (Refer to Figure S-2).

3.1 Start without input AC power (Cold start):

A "Cold start "is described as follows:

3.1.1 When "ON/OFF" switch (SW1) is pressed, a positive battery current flows through SW1 to charge C11.

3.1.2 Q8 base receives a HI pulse and turn on (signal bypass C11 at t=0, and charge C11 at t>0).

3.1.3 When Q8 turns on, the Q8 collector will drop to LOW and turn on Q6 (MPS2907A).

3.1.4 When Q6 turns on, the positive battery voltage will activate U2 (PWM IC 3845) through Q6, R36 and D8. When U2 starts to work, it will generate PWM signal to control Q7, and this will establish a ±12Vdc and ±6V-BLN through fly-back transformer TX2. The +12Vdc power supply passes through U1 (78L05) generating a +5Vdc logic power supply.

3.2 Start with input AC power (AC start):

3.2.1 When we connect UPS to the utility, full-wave rectifier will activate Q8 through ZD1, U3 and Q10.

3.2.2 If "ON/OFF" switch is pressed, Q6 turns on and establishes a +12Vdc and +5Vdc power supply similar to "Cold start".

The SD network, triggered by pin 60 of the CPU, is used to shut down the UPS on battery mode. When a battery is in low battery voltage status, the CPU sends a "high" signal to turn on Q9. This causes pin 1 of U2 to drop to LOW. U2 will be turned off and isolates the control power from batteries.

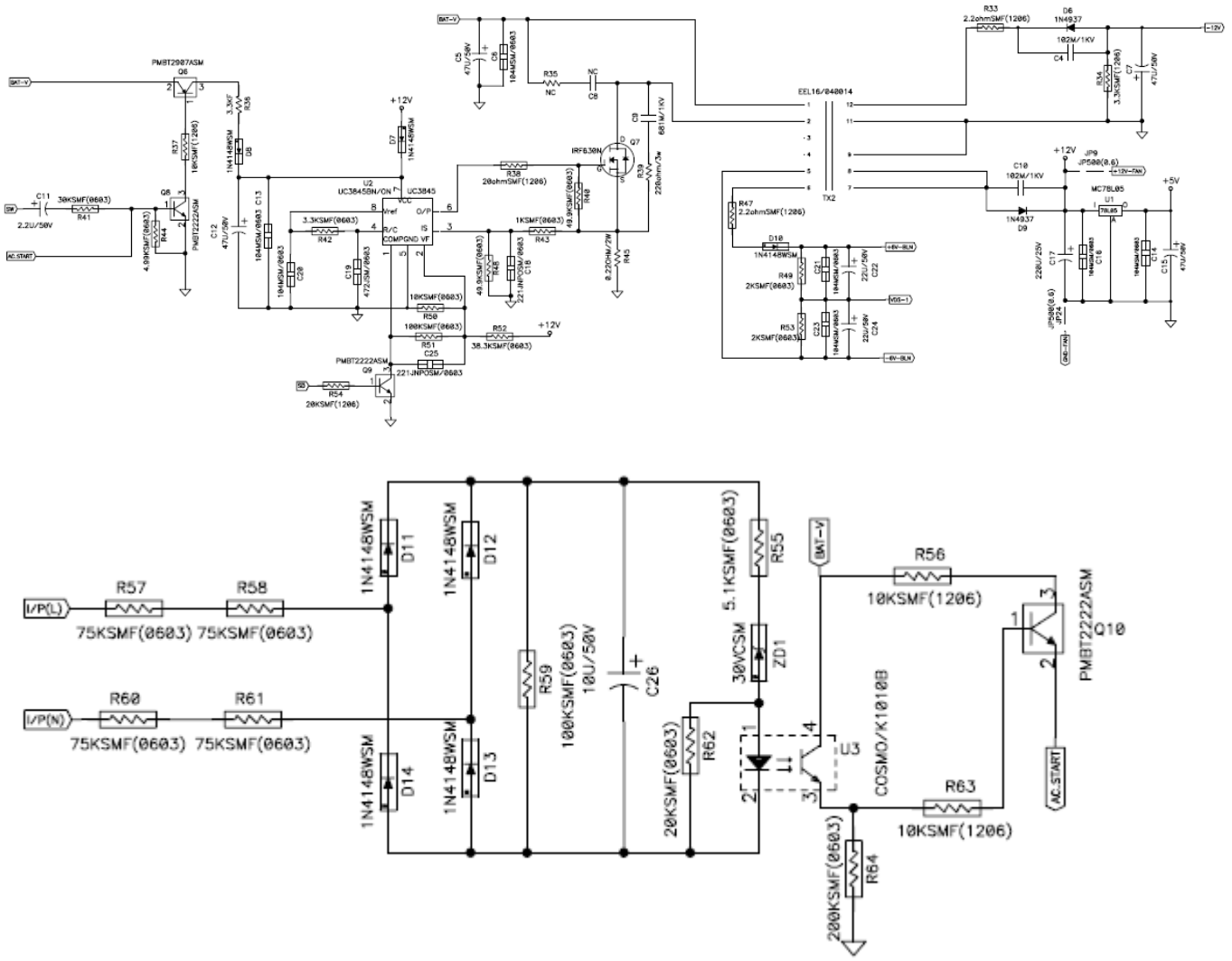


Figure S-2: control power circuit diagram

4 Battery Charger

The flow chart of charger is described as follows: (Figure S-3-A & Figure S-3-B)

4.1 When UPS is connected to the utility, the control power (+5Vdc) will be established and the CPU will start to work.

4.2 When CPU turns on Main Relay (RY1 & RY5), the AC power flows into Main Transformer.

4.3 Charging current will be generated from the inverter coil of the Main Transformer.

4.4 A PWM IC 3843 is used to adjust the charging voltage and charging current. (Refer to Figure S-3-A) The charging voltage can be set by changing the value of R99, R105, R100 and R106. The charging current can be set by changing the value of R101.

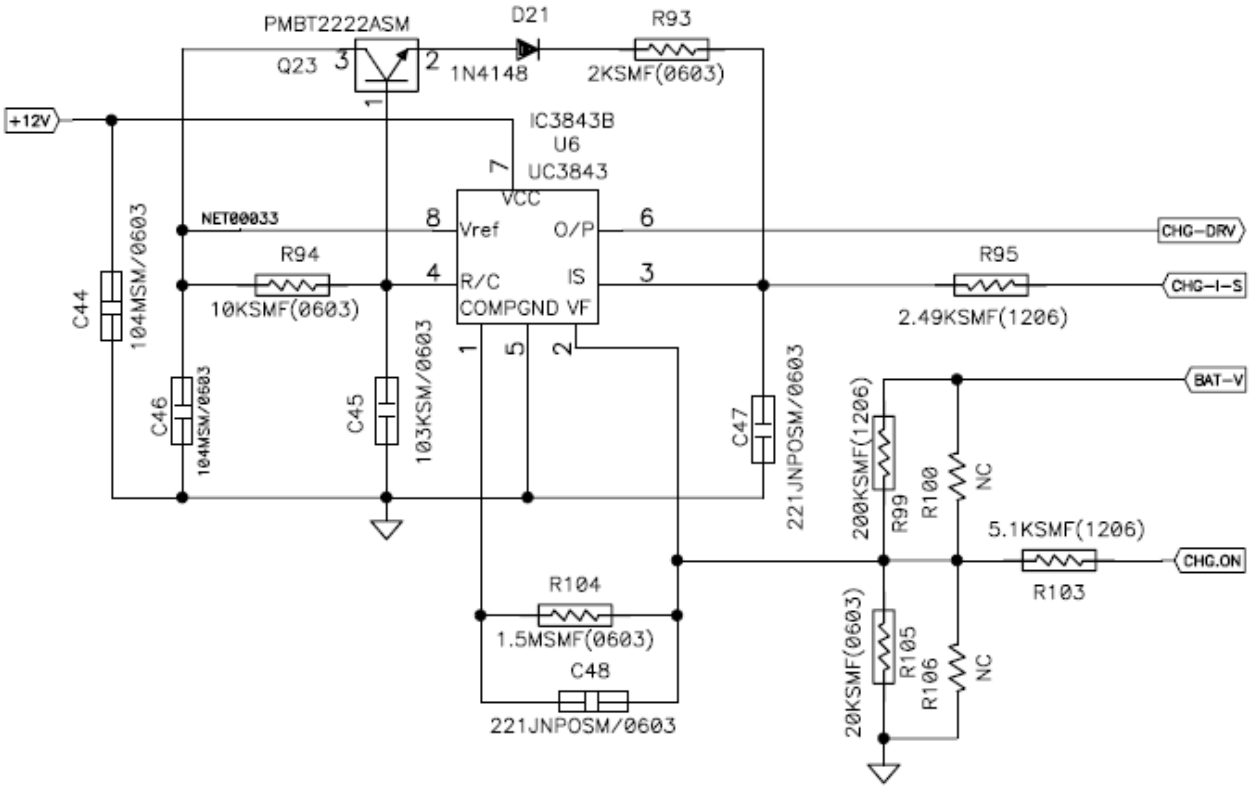


Figure S-3-A Charger Control Circuit

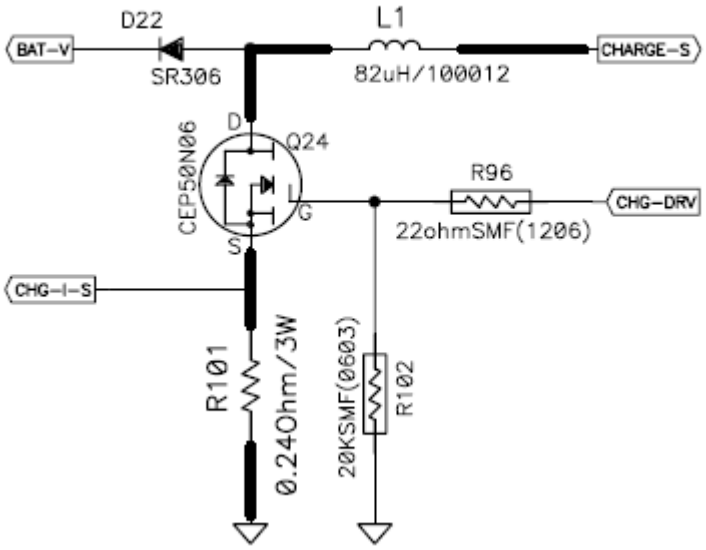


Figure S-3-B Charger Control Circuit

5 Line and Zero-Crossing Detection

Please refer to Figure S-4

5.1 Line Detection on control board

The input voltage is fully rectified and generates a signal. The signal will be sent to pin 34 of CPU through a voltage divider at R63, R59, R68 and R73. By monitoring this rectified sinusoidal voltage, the CPU can identify if the utility is normal or abnormal. There are two methods to evaluate if line voltage is abnormal.

5.1.1 Waveform detection:

If breakout occurs, the CPU is able to immediately detect it and transfers to battery mode. The waveform detection has a short response time.

5.1.2 RMS value detection:

CPU calculates input RMS value every cycle. If RMS value is not in acceptable range for 3 cycles, UPS will transfer to battery mode. Compared to waveform detection, although it will take longer response time, the RMS value can be accurately detected.

5.2 Zero Crossing Detection

Zero Crossing Detection is used to minimize the phase difference between the Inverter voltage and the input line voltage while UPS is switched from battery mode to line mode. If the phase difference is too large, it will generate excess energy which may damage the internal passive components such as relays.

The Zero Crossing signal is generated by the following conditions:

5.2.1 The signal of Line-I/P is full-bridge rectified waveform from line input. The voltage of Pin 7 in IC324 drives Q4 (2222ASM) on or off.

5.2.2 The Zero Crossing signal comes from the Q4 collector and goes through pin 4 of MCU.

5.2.3 Refer to Figure W-2. The waveform of ZERO-CRO from Q4 collector and Line-I/P.

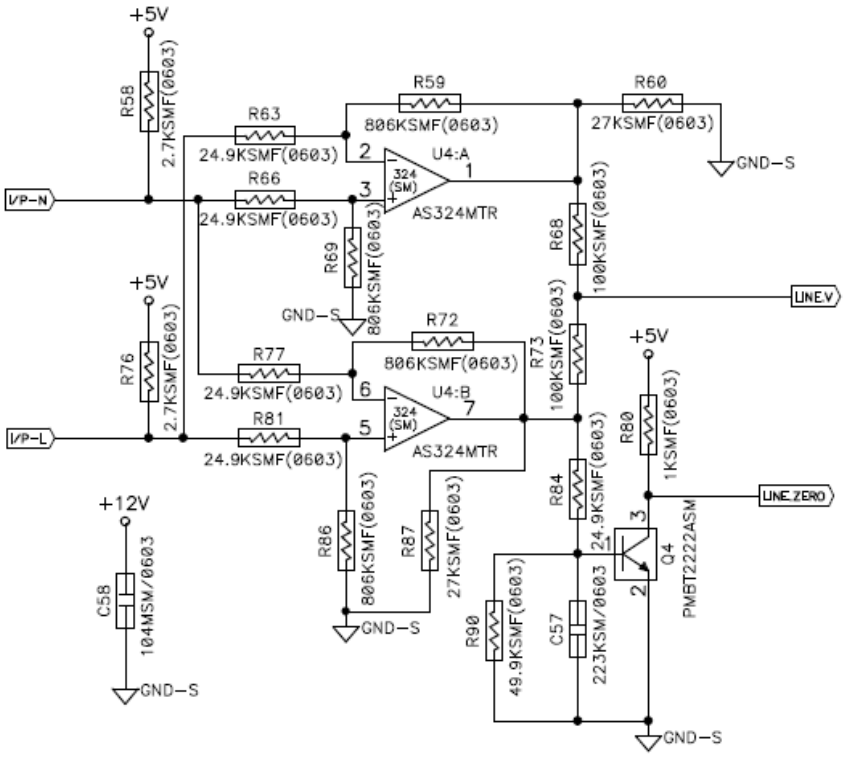
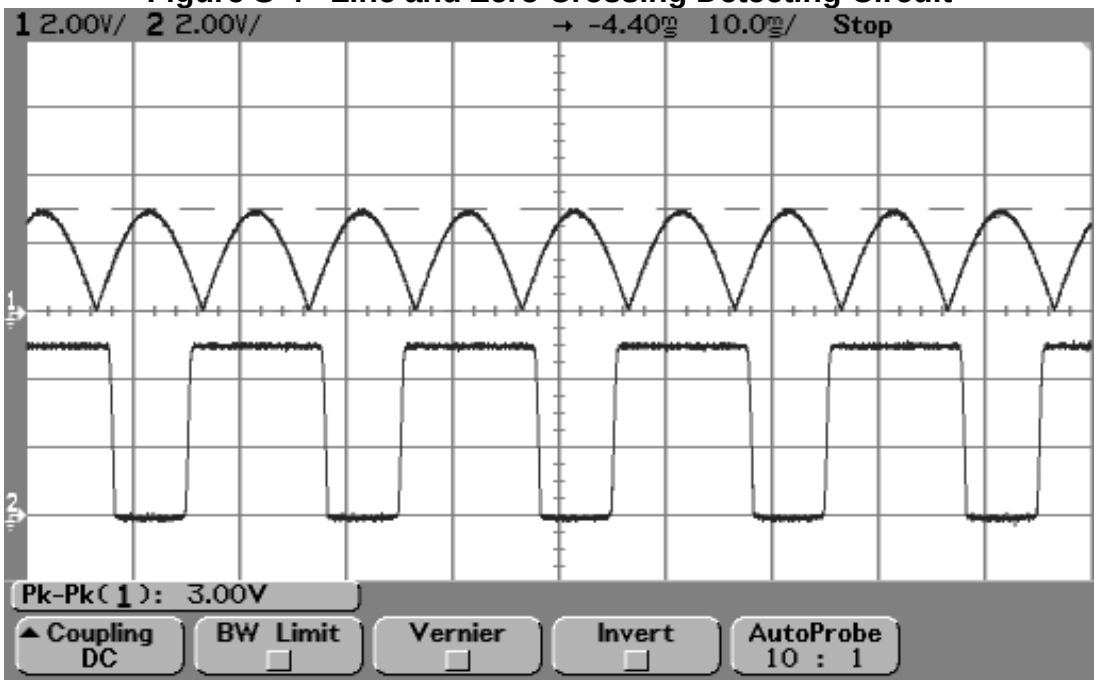


Figure S-4 Line and Zero Crossing Detecting Circuit



CH1: Line-I/P
CH2: Q4 collector

Figure W-2 Zero Crossing

6 Inverter Operation

The Inverter circuit (Figure S-5) and PWM control are only active under Battery mode. The Inverter circuit of LP120is based on a full-Bridge circuitry and its output is driven by a PWM IC IR2104. The IR2104(s) are capable to drive high energy and high speed power of MOSFET and IGBT with independent high and low referenced output channels. The high channel of U4 is to drive Q13&Q11; and the low channel is to drive Q17&Q19. These two signals are opposite at the same time. And the high gate driver is in phase with input logic.

Refer to the Inverter circuit diagram. “IN3.SD” is to shut down U4&U5. That means it will shut down output inverter. Input logic of U4—“PWM2” and U5—“PWM1” is generated by “PWM control circuit” (Figure S-6),

There are two important parts in “PWM control circuit”. One is output voltage feedback circuit (Figure S-6-part 1); and the other is sine reference generating circuit (Figure S-6-part 2). PWM signal generated by CPU transforms to sine reference signal via PI controller. Error signal will be generated from PIN 8 of U9 after comparing sine reference signal and output voltage signal through differential comparator U9:C. Then, with differential comparator U5: B, it will compare triangular wave (from PIN 11 of CPU) and error signal to generate a high frequency PWM control signal, PWM1. In the other hand, error signal is also used to generate 50Hz PWM control signal, “PWM2”.

Figure W-3 (1) shows the collector waveforms for CPU while the system is at different conditions.

These inverter transistors are turned on and off alternately to transfer DC battery voltage to an AC step wave output voltage, and then magnifies through the transformer and output capacitance C1 to generate a stable sine wave output, which voltage is 230VAC

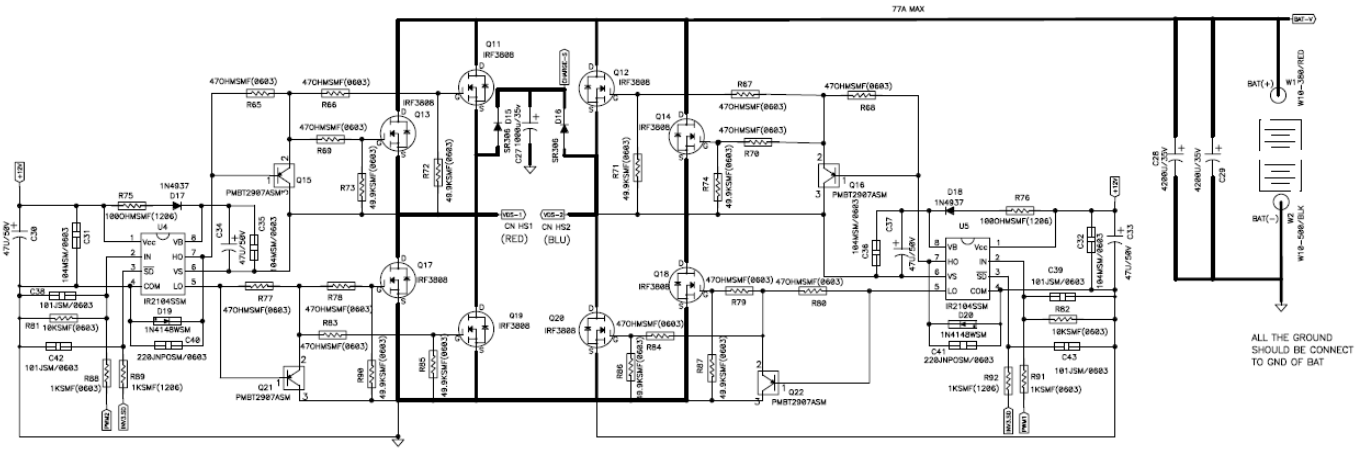


Figure S-5 Inverter circuit

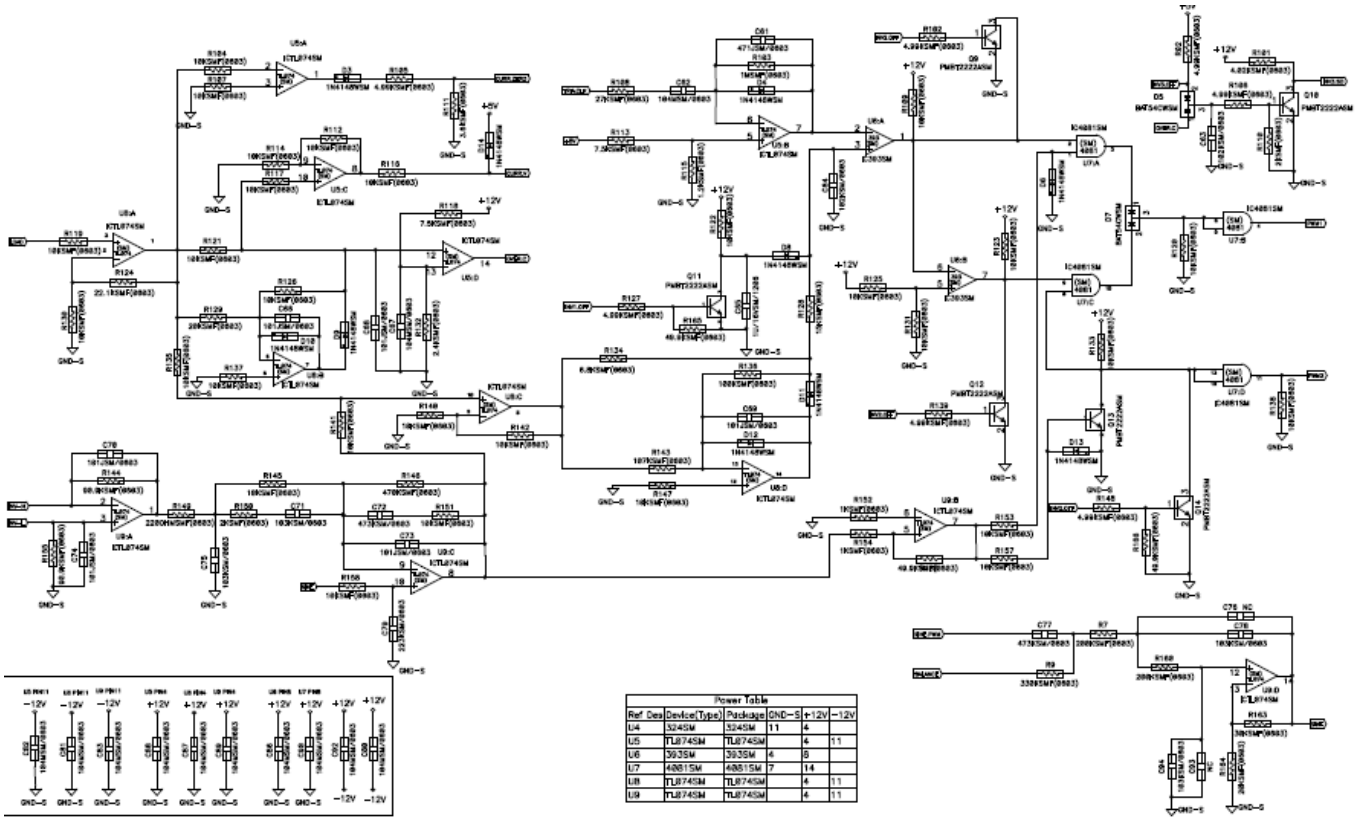


Figure S-6 PWM control circuit

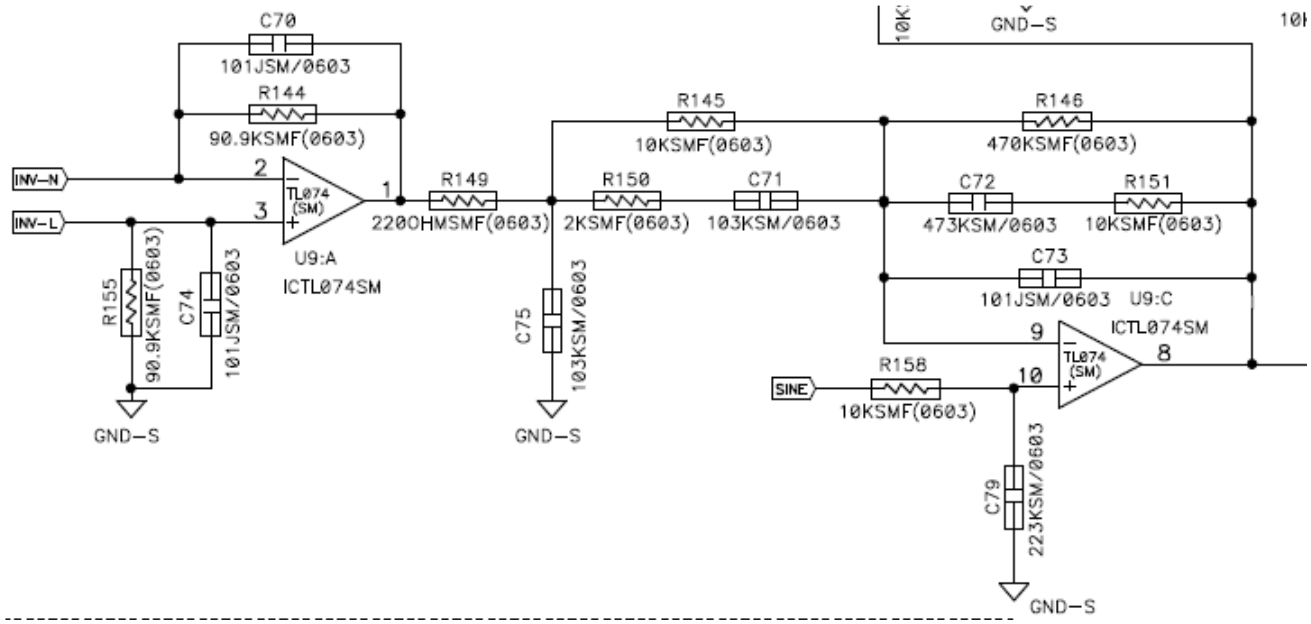


Figure S-6-part 1

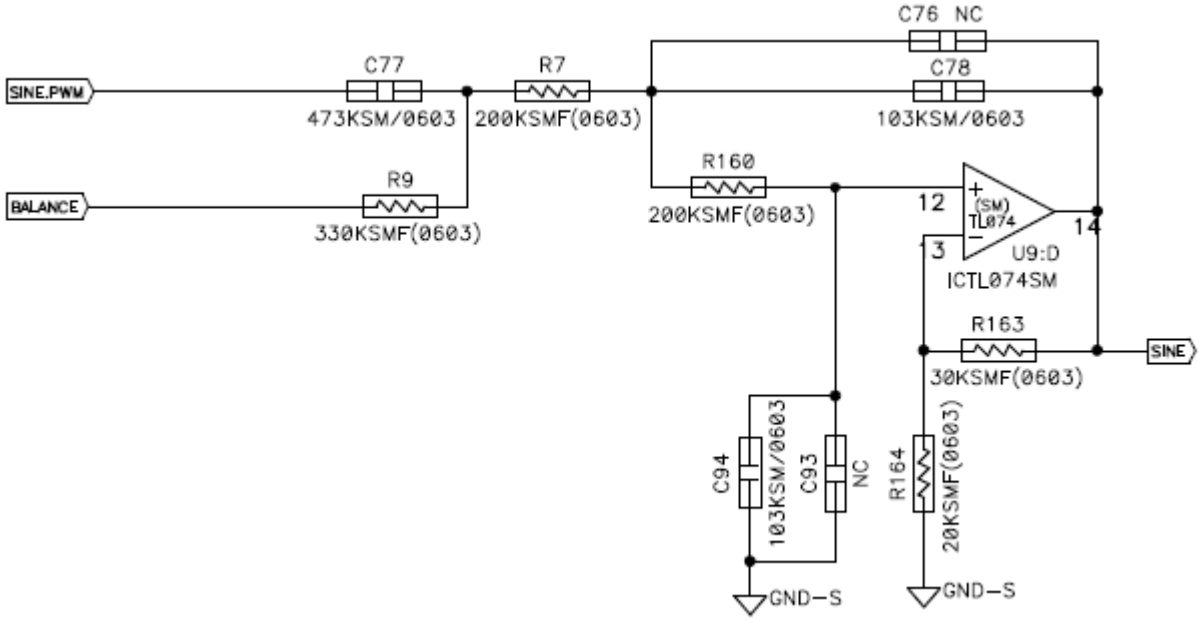


Figure S-6-part 2

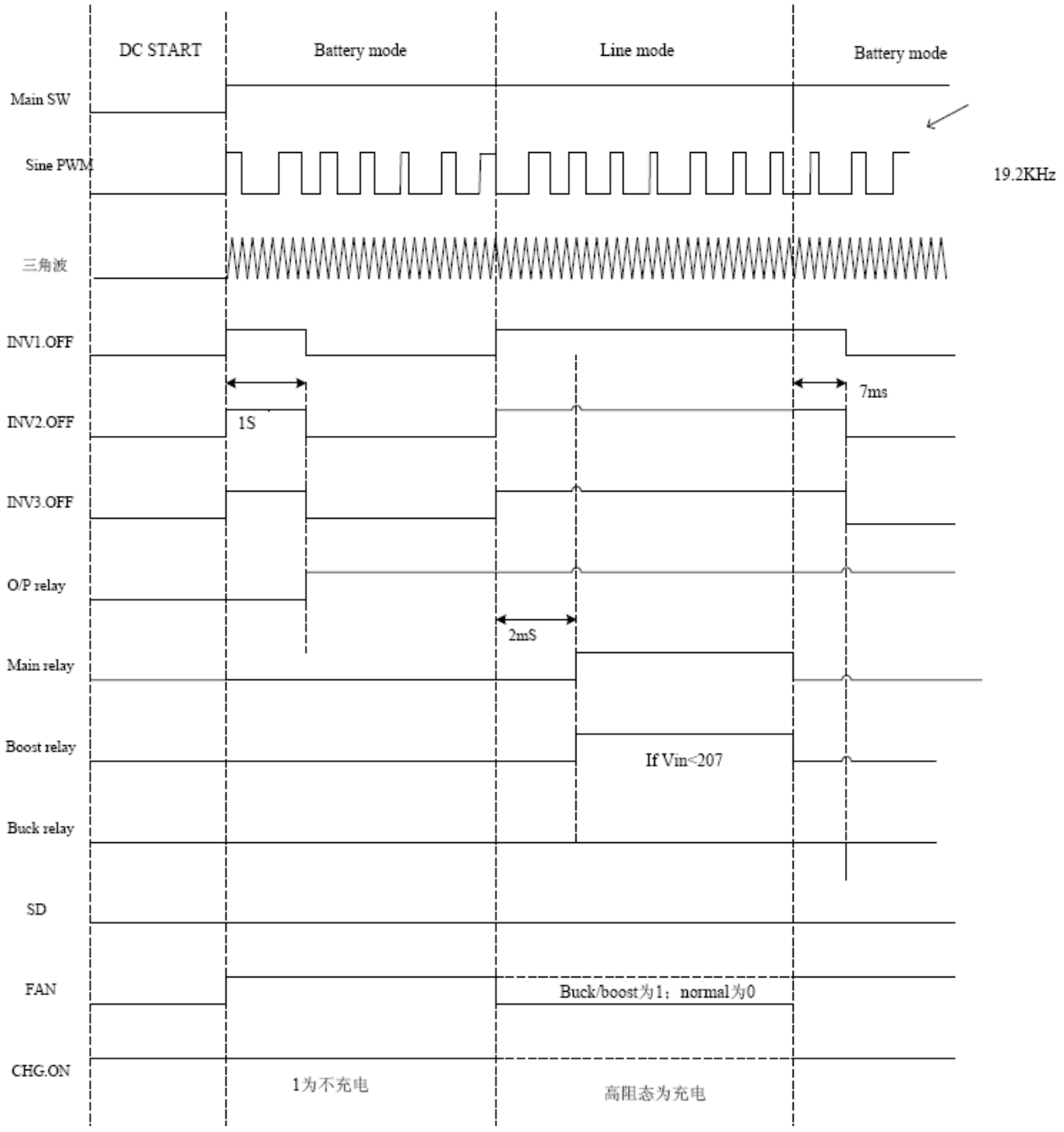


Figure W-3 Control logic (1)

7 Microprocessor(CPU) Control Circuit

The CPU is supplied by +5Vdc power supply to pin22 with ground pin at pin21. An extra oscillation circuitry consisting of C29, C32, and crystal XL1 is connected to pin58 &57. The LP120series is using PREESCALE/ MC9S08AC48 CPU. The pin definition is listed below (Figure S-6):

Pin name	PIN No	Functionality	Name	Type	Action
PTC4	1	GPIO	MAIN.SW	Input	High
IRQ/TPMCLK	2	External interrupt	IRG	Input	High
RESET	3	CPU reset	RESET	Input	Low
PTF0/TPM1CH2	4	Input capture	LINE.ZERO	Input	Falling Edge
PTF1/TPM1CH3	5	Input capture	CURR-ZC	Input	Falling Edge
PTF2/TPM1CH4	6	Input capture	INV.ZERO	Input	Falling Edge
PTF3/TPM1CH5	7	GPIO	BUZZER.ON	Output	High/LOW
PTF4/TPM2CH0	8	PWM	SINE.PWM	Output	High/Low
PTC6	9	GPIO	CHG.ON	Output	High- High impedance
PTF7	10	GPIO	CHG.COST_I	Output	High
PTF5/TPM2CH1	11	PWM	TRIA.CLK	Output	High/Low
PTF6	12	GPIO	CONVERT OFF	Output	Low
PTE0/TxD1	13	SCI Transmit 1	TXD1	Output	High/low
PTE1/RxD1	14	SCI Receive 1	RXD1	Input	High/low
PTE2/TPM1CH0	15	GPIO	FAN1.ON	Output	High
PTE3/TPM1CH1	16	GPIO	FAN1.CLK	Input	High/Low
PTE4/SS1	17	GPIO	BUCK.RLY	Output	High
PTE5/MISO1	18	GPIO	BST.RLY	Output	High
PTE6/MOSI1	19	GPIO	INV.RLY	Output	High
PTE7/SPSCK1	20	GPIO	MAIN.RLY	Output	High
V_{SS}	21	Core GND	VSS		
V_{DD}	22	Core VDD	VDD		
PTG0/KBI1P0	23	GPIO	STS.ON	Output	High
PTG1/KBI1P1	24	GPIO	DATA	Output	High/Low
PTG2/KBI1P2	25	GPIO	CS/DATA.CLK	Output	High/Low
PTA0	26	GPIO	WR/DATA.EN	Output	High
PTA1	27	GPIO	NC	Output	Low
PTA2	28	GPIO	NC	Output	Low
PTA3	29	GPIO	NC	Output	Low
PTA4	30	GPIO	NC	Output	Low
PTA5	31	GPIO	NC	Output	Low
PTA6	32	GPIO	NC	Output	Low
PTA7	33	GPIO	NC	Output	Low
PTB0/TPM3CH0/AD1P0	34	AD	LINE.V	Input	Analog
PTB1/TPM3CH1/AD1P1	35	AD	INV.V	Input	Analog
PTB2/AD1P2	36	AD	BAT.V	Input	Analog
PTB3/AD1P3	37	AD	TEMP1.V	Input	Analog
PTB4/AD1P4	38	AD	CURR.V	Input	Analog

PTB5/AD1P5	39	AD	MODEL0	Input	Analog
PTB6/AD1P6	40	AD	MODEL1	Input	Analog
PTB7/AD1P7	41	AD	MODEL2	Input	Analog
PTD0/AD1P8	42	AD	MODEL3	Input	Analog
PTD1/AD1P9	43	AD	TEMP2.V	Input	Analog
V_{DDAD}	44	AD VDD	VDDAD		
V_{SSAD}	45	AD GND	VSSAD		
PTD2/KBI1P5/ AD1P10	46	GPIO	BATMODE	Output	High
PTD3/KBI1P6/ AD1P11	47	GPIO	BATLOW	Output	High
PTG3/KBI1P3	48	GPIO	REMOTE.SD	Input	High
PTG4/KBI1P4	49	GPIO	INV1.OFF	Output	Low
TPD4/TPM2CLK/AD1P 12	50	GPIO	INV2.OFF	Output	Low
PTD5/AD1P13	51	GPIO	INV3.OFF		Low
PTD6/TPM1CLK/AD1P 14	52	GPIO	FAN2.ON	Output	High
PTD7/KBI1P7/ AD1P15	53	GPIO	FAN2.CLK	Input	High/Low
V_{REFH}	54	AD REF HIGH	VREFH		
V_{REFL}	55	AD REF LOW	VREFL		
BKGD/MS	56		PROG		
PTG5/XTAL	57	Crystal Input	XTAL	Input	To Crystal
PTG6/EXTAL	58	Crystal Output	EXTAL	Output	To Crystal
V_{SS}	59	Crystal GND	VSS		
PTC0/SCL1	60	GPIO	SD	Output	Low
PTC1/SDA1	61	GPIO	NC	Output	Low
PTC2/MCLK	62	GPIO	FUN1.RLY	Output	High
PTC3/TxD2	63	GPIO	FUN2.RLY	Output	High
PTC5/RxD2	64	GPIO	PNP	Input	High/Low

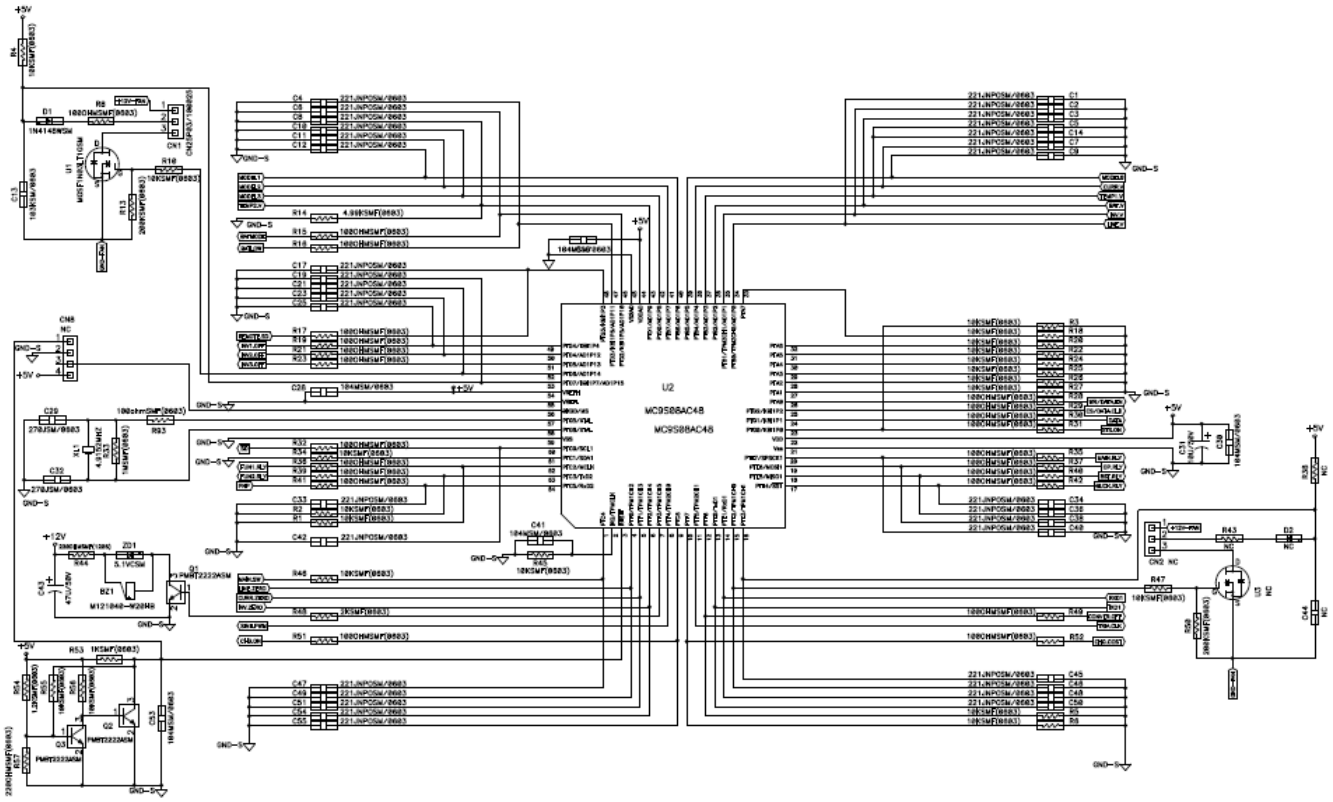


Figure S-6 CPU Control Circuit

8 Relay Circuit

Figure S-7 is the relay circuit.

RY1 & RY5 (main relays) are used to switch between line mode and battery mode. When the UPS is transferring from battery mode to line mode, CPU pin20 is set to HI to turn on Q2 and activates RY1 & RY5. Alternatively, if the UPS is transferring from line mode to battery mode, CPU pin20 is set to LOW and turn off Q2. This causes RY1 & RY5 to be OFF and return to its normal state.

R6, D1, C3 and Q1 are used to speed up the relay transfer action, so the power failure time can be shorten to minimum. When UPS transfers to battery mode, C3 is charged by the +12 Volts. After the main relay makes contact, C3 provides instantaneous power to the relay coils. This will increase the magnetic force and shorten the transfer time from battery mode to line mode by switching the relay.

CPU pin18 is used to drive signal for RY4 (boost relay). When the mains input voltage is low as within boost activated point, pin18 sends a high signal to turn on Q5. This will activate the RY4, and UPS will transfer to the Boost mode. When the mains input voltage increases back to reach inactivated boost point, the UPS will return to normal mode by sending a LOW signal from pin18. This forces RY4 to switch to its normal position (OFF). At battery mode, pin18 is always set to LOW and RY4 is disabled.

Buck situation will apply for the similar process. CPU pin17 is used to drive signal for RY3 (buck relay). When the mains input voltage rises beyond buck activated point, CPU pin17 sends a high signal to turn on R3. When the mains input voltage drops to lower than the inactivated buck point, the UPS returns back to normal mode by sending a LOW signal from pin17.

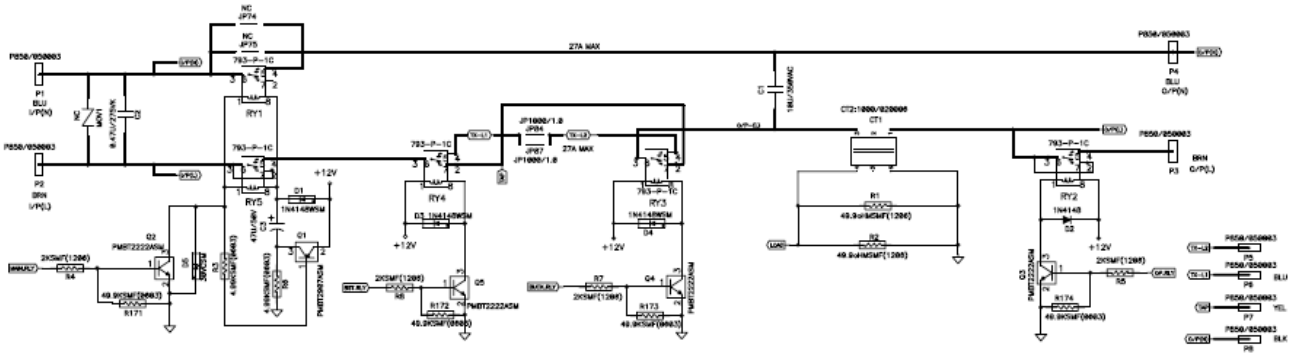


Figure S-7 Relay Circuit

9 Displays, Audio Alarm and Control Button

9.1 Control button

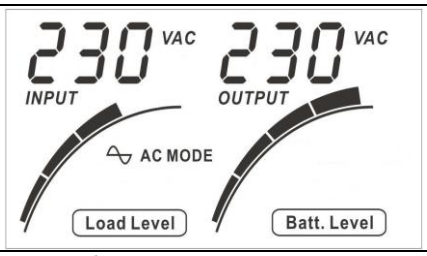
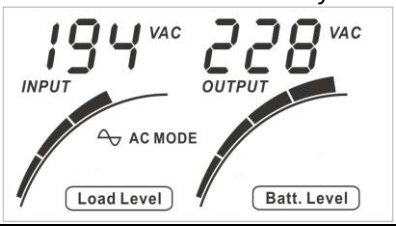
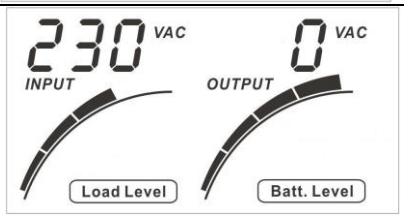
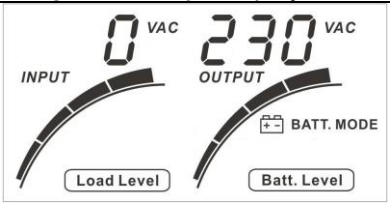
ON/OFF Button: Push it to turn on UPS, and push again to turn off UPS.
(Please refer to Chapter 3 for cold start & AC start)

9.2 Audio alarm

The buzzer is controlled by pin7 of CPU. When CPU sends a HI signal to buzzer from pin7, buzzer is beeping. And CPU sends LOW signal to stop buzzer.

9.3 Display (Figure S-8)

There is a LCD on the front panel.
When control button is pressed, CPU sends signals to highlight the LCD.

MODE	SPEC
	1 LCD
- AC Mode	
- AVR Mode	The icon AC MODE will flash every second. 
- Off-mode charging	 . Note: The output voltage will always display “0” at off-mode charging.
- Battery Mode	 Note: If input voltage is lower than 40V, it will display “0” in input voltage.

- Fault mode	
- Overload	The mark  will flash every second.
- Low battery	The mark  will flash every second.

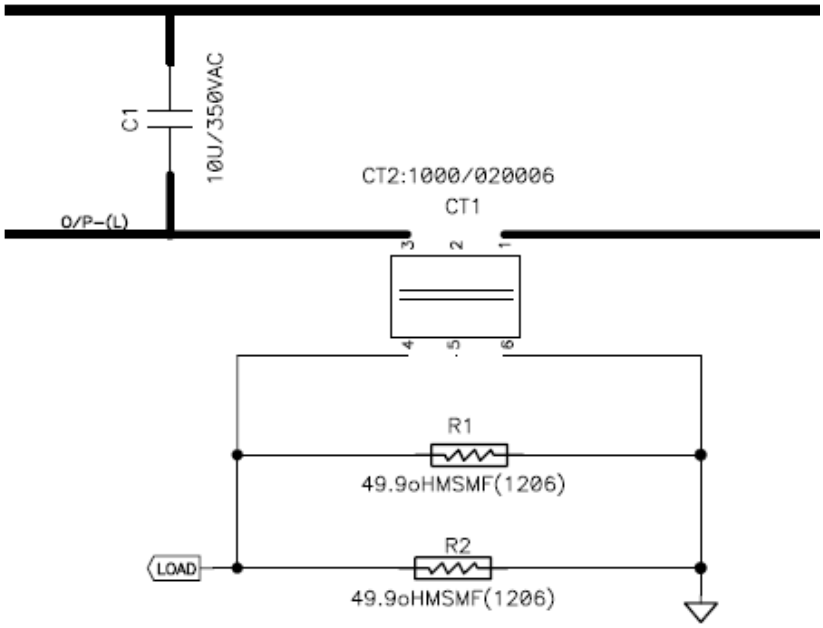
Figure S-8 Display of LCD

10 Load Detection Circuit

Load detection circuit is shown on Figure S-9. The output current is detected by current transformer CT1. It lowers 500 times of output current for CPU detection. The current signal generated from CT1 flows through R1 & R2 to convert to a voltage signal. The voltage signal turned into two signal: one is “CURR.V”, another is “CURR.ZERO”, and sent to CPU through an operational amplifier U5. “CURR.V” (0~5 Volts) shows current value. “CURR.ZERO” shows phase of current. CPU can calculate value of “W” and “VA” from these two data.

10.1 At line/boost/buck mode: The current value multiplies output voltage to get output VA value.

10.2 At battery mode: Because the power factor of step wave is approximately equal to 1, the current value multiplies 120V (230V) output voltage to get output Watt value.



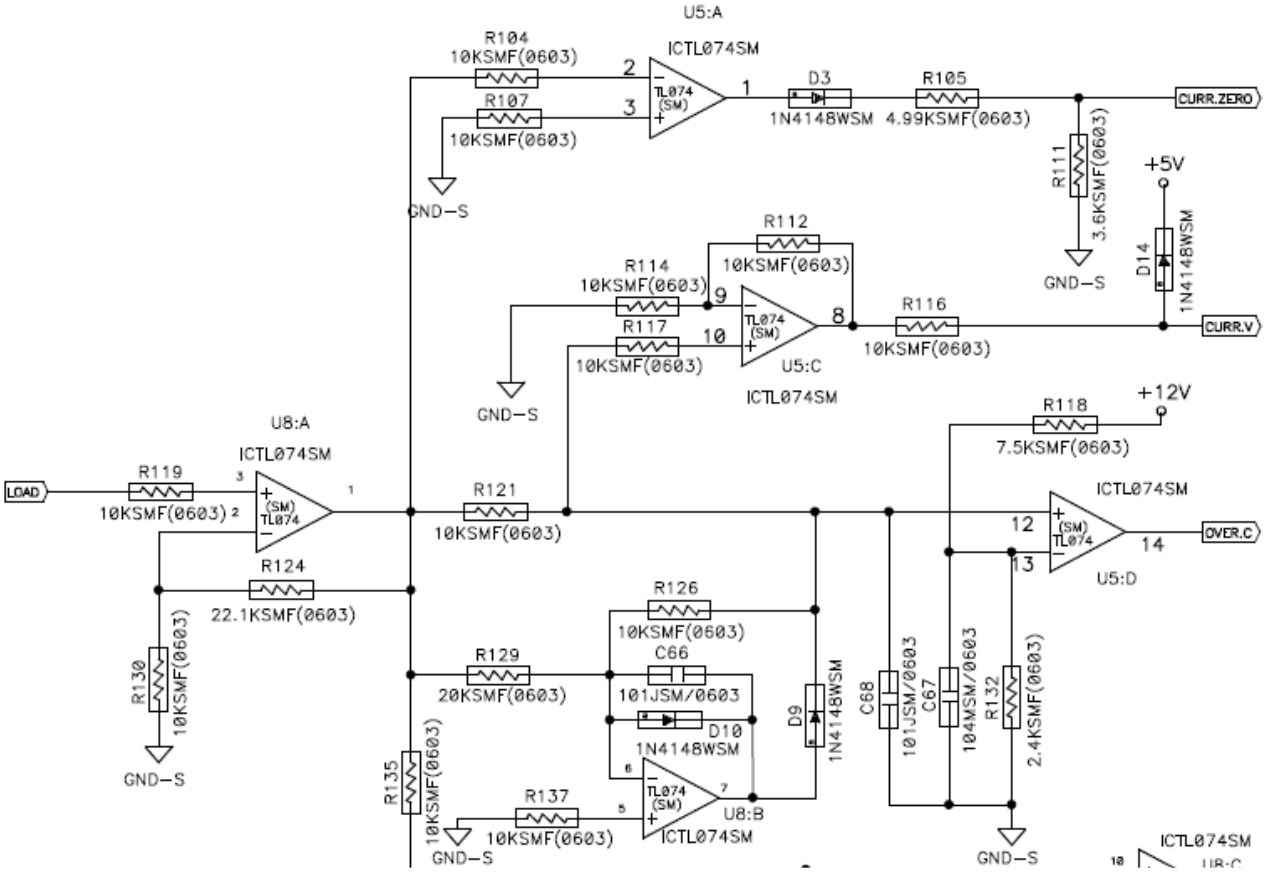


Figure S-9 Load Detection Circuit

11 Interface Circuit

Please refer to Figure S-10 as USB interface circuit and plug & play for Windows 95/98/2000/XP/NT.

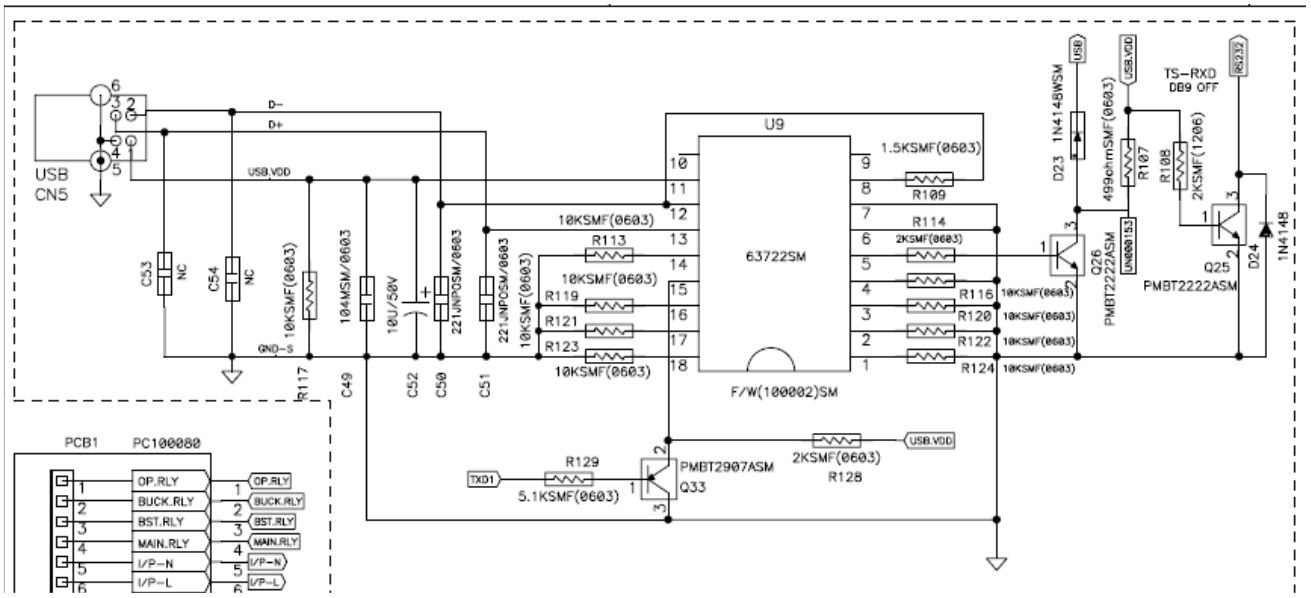


Figure S-10 USB Interface Circuit

12 Troubleshooting

WARNING

12.1 Troubleshooting can be done by qualified engineer or technician only.

12.2 Use isolated AC source for your oscilloscope to prevent floating voltage problem between UPS chassis ground and system reference ground.

12.3 Before opening the cover, turn off the main switch and unplug the input power cord.

12.4 Because hazardous voltage may remain in the DC capacitors, wait for at least 5 minutes after turning off the UPS and disconnecting the power cord before open its cover.

12.5 Do NOT plug in the input power cord before you reconnect the connectors of battery to prevent unwanted sparks.

Please follow the steps below when you want to repair a problematic unit:

12.6 Visual inspection

This is the first step to check the UPS after opening its cover. Be sure to do the visual inspection because it can help you to identify most problems. Major items that should be checked are listed below:

12.6.1 Are there any connectors or terminals loose?

12.6.2 Is there any components burn-out or discolored?

12.6.3 Especially the power components on the heat sink?

12.6.4 Are there any capacitors broken or leakage? Check all the components listed above and replace which is abnormal.

12.7 Troubleshooting flowchart

To prevent from hurting yourself and damaging the UPS, be sure to obey the sequences of flowchart listed below.

12.7.1 Battery mode examination (please refer to Figure W-7)

Procedure:

For main power board:

1. Replace batteries by DC power supply and turn on it. Check if there is current limit phenomenon for DC power supply.
2. One or more MOSFET(s) (Q11~Q14, Q17~ Q20) is D-S short. Check and replace it. If MOSFET(s) have been replaced once, replace the PCB.
3. Check if there is current limit phenomenon for DC power supply.
4. Check if R65~R74; R77~R80; R83~R87; R90 is OK.
5. Replace abnormal R65~R74; R77~R80; R83~R87; R90
6. Check if Q15, Q16, Q21, Q22 is OK.
7. Replace abnormal Q15, Q16, Q21 and Q22.
8. Check if D15, D16, D22 is OK,

9. Replace abnormal D15, D16 and D22
10. Check if Q24 is D-S short
11. Replace abnormal Q24.
12. Check if PWM signal of U4 & U5 is OK. The high gate drive signal is opposite with low gate drive signal. And the high gate driver is in phase with input logic. Replace abnormal U4 & U5. If they have been replaced once, replace the PCB.
13. Check if both buzzer beeps and LCD flash for one time
14. Check if there is +12Vdc on regulator U1 (7805) input.
15. Check if +5Vdc on U1 (7805) pin 3 is normal.
16. Check if Q7 is D-S short
17. Replace abnormal Q7
18. Check if there is PWM control signal to drive Q7
19. Check if there is high pulse voltage on PIN 7 of U2 (3845) when pressed on button
20. Check Q6 (MPS2907A), Q8 (2222ASM) is OK
21. Replace abnormal transistors
22. Check if there is concussion signal on PIN 4 of U7
23. Replace abnormal C19、C20、R42 or U2
24. Check if there is +12Vdc on 7805 input.
25. Replace abnormal TX2
26. Check if there is +5Vdc on 7805
27. Replace abnormal 7805
28. Check if +5Vdc is short with negative pole of battery on MAIN POWER BOARD
29. Check if CN7 PIN1 (+5Vdc) is short with PIN5 (GND-S) on LCD display.
30. Replace LCD display
31. Cut JP7, Check if +5Vdc is short with negative pole of battery
32. Replace CONTROL board
33. Replace total PCB
34. Check if battery voltage is incorrect.
35. Replace abnormal batteries.

12.7.2 Line mode examination (please refer to flowchart Figure W-8)

If battery mode examination is OK, then do the line mode examination as below.

12.7.2.1 Plug in input power cord at right voltage range. Check if main relay RY1& RY5 is active.

12.7.2.2 Replace main relay.

12.7.2.3 Check Q4 (2222ASM collector on CONTROL BOARD) if there is zero crossing signal.

12.7.2.4 Replace abnormal Q4. Check if UPS remains on line mode.

12.7.2.5 Replace PCB.

12.7.2.6 Check if buzzer beeps continuously and fault LCD lights.

12.7.2.7 Check if Buck/Boost relays (RY4, RY3) are bad.

12.7.2.8 Replace abnormal Buck/Boost relays (RY4, RY3).

12.7.2.9 Replace PCB.

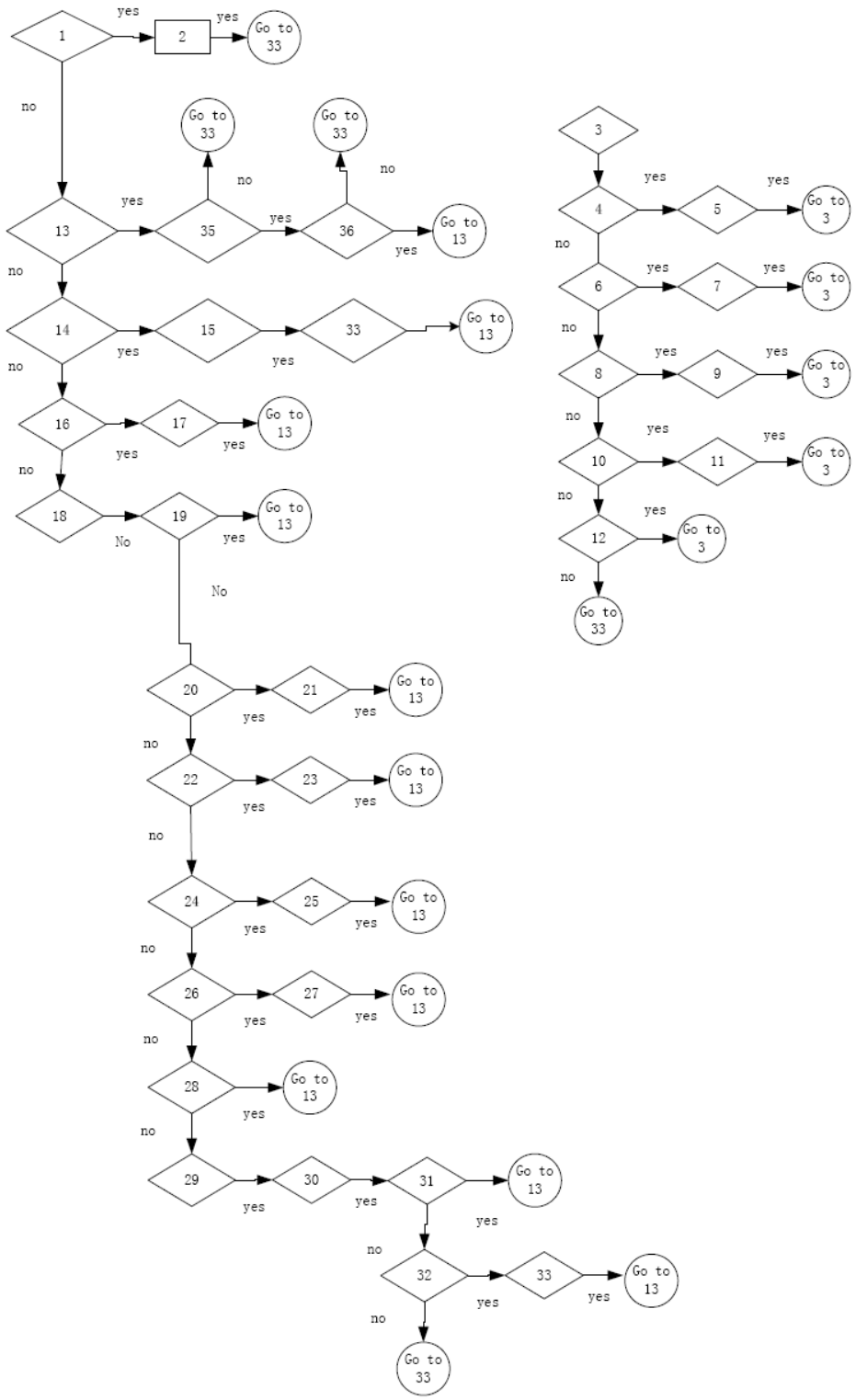


Figure W-7 Battery Mode Examination Flowchart

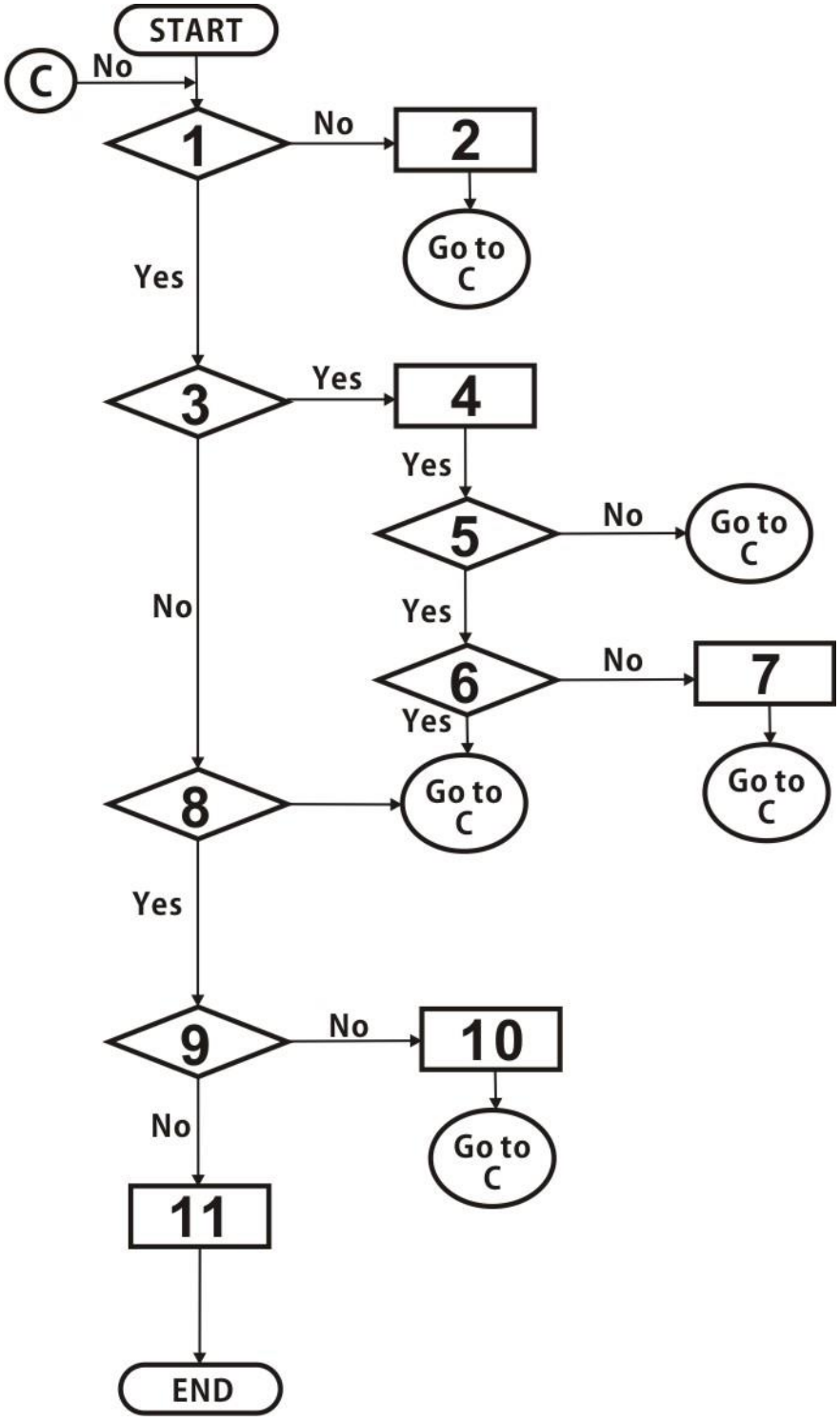


Figure W-8 Line Mode Examination Flowchart